REMARKS

This paper amends the specification and Claims 9, 11, 18-21, 25 and 29, cancels Claims 12 and 30, and adds new Claims 32-37. Claims 1-8, 10, 13-17, 22-24, 26-28 and 31 are unchanged. Claims 1-11, 13-29 and 31-37 are pending. Reconsideration and allowance of the claims in light of the present remarks is respectfully requested.

Discussion of Amendment to Drawings

Applicant has amended Figure 2 as shown in the Replacement Sheet for Figure 2. Specifically, the legend –Prior Art– is added as requested by the Examiner.

Discussion of Rejection under 35 U.S.C. § 112, first paragraph

Applicant respectfully submits that the corrections made in the substitute specification mailed on June 21, 2002 are not the basis for any claim limitations. For example, Claim 1 is supported by the description at page 15, line 23 to page 19, line 29 of the specification as originally filed. The corrections were made primarily to clarify the specification, correct clerical errors and conform the figures to the specification. However, in response to the Examiner's comments, Applicant has restored portions of the patent specification as originally filed and has provided comments regarding other portions of the specification.

The change to the title was made in the substitute specification to more accurately describe the invention. The specification was amended to correspond the figure numbers in the specification with the figures.

The specification includes changes that reflect the change in number of figures, correction of typographical errors, and the like. Some of the clarifications are to make portions of the detailed description consistent with other portions of the detailed description. Several specific passages are discussed as follows. At page 14, lines 4-6 of the "compare" version of the specification that was referred to by the Examiner, Applicant has restored the specification to end the sentence after the term "constraint" (line 4). At page 20, line 20, an example such as described at page 25, line 4 was added. At page 21, line 19, the change corrects an apparent typographical error. Line 17 describes a slack of -2, -1 so lines 18- 19 should match line 17 so

that it is stated that -1 is processed first and … -2 is the last to be processed. At page 25, line 5, the added word "next" is described on page 20, lines 17-22.

Discussion of Rejection under 35 U.S.C. § 102(b) and § 103(a)

Claims 1-14, 18-21 and 25 are rejected under 35 U.S.C. § 102(b) as being anticipated by Singh (Singh, K.J., "Performance Optimization of Digital Circuits, Ph.D. Dissertation, University of California Berkeley, 1992), referred to as Singh '92. Claims 29-31 are rejected under 35 U.S.C. § 102(b) as being anticipated by Singh et al. (Singh et al., "Timing Optimization of Combinational Logic," Computer-Aided Design, 1988. ICCAD-88. Digest of Technical Papers, IEEE International Conference, 7-10 Nov. 1988, Pages 282-285) referred to as Singh '88. Dependent Claims 15-17, 22-24, and 26-28 are rejected under 35 U.S.C. § 103(a) as being obvious over Singh '92 as applied to Claims 11, 21 and 25, and further in view of applicant's own admission. According to the Examiner, applicant's own admission was identified as one sentence on page 1 of the patent specification as follows: "As timing problems become more and more crucial in integrated circuit (IC) designs, timing-driven logic resynthesis is often needed at various design stages to minimize circuit delays."

Applicant's **Claim 1** includes novel ordering techniques. These ordering techniques are not used in Singh '92. During each iteration, Singh '92 selects multiple nodes to do local transformations at one time and performs transformation on all these nodes together, ignoring the fact that transforming one node likely leads to the unnecessary transformation of another node in the transformation set.

Applicant respectfully submits that the citation of page 48-49 of Singh '92 does not describe "sorting fanins of the first node according to slack values associated with the corresponding fanins, wherein at least a portion of the slack values differ in value." The Examiner identified the description of ε-critical network and Figure 3.7 as describing this element. The Singh reference states that "the ε-critical network consists of all the nodes and edges in the Boolean network that have a slack within ε of the minimum slack (ε is a user specified constant)". This description and the node network diagram shown in Figure 3.7 do not describe sorting fanins of the first node according to slack values associated with the corresponding fanins.

Applicant respectfully submits that the citation of page 50-51 (Proof) of Singh '92 does not describe "reducing delays associated with fanins having relatively larger negative slack values before reducing delays associated with fanins having relatively smaller negative slack values." The proof cited at page 50 of Singh '92 proves a way to determine the maximum improvement and does not disclose the claimed ordering technique. The Singh '92 reference does not describe that there is a preference for which fanin to choose first, because the entire approach or framework is different. Singh describes computing a set of transformations first and then applying the transformations. In contrast, Applicant computes transformations dynamically, which is why there is an ordering.

Advantages of Applicant's claimed method are as follows. As described at least on pages 16-19 of the originally filed specification, the fanin pin (and its fanin logic cone) with the largest (negative) slack meets timing requirements (getting to zero or positive slack) more easily than the fanin pin with a smaller (negative) slack. If the fanin pins for which it is easier to meet timing cannot reduce delays to meet the timing, the method terminates and moves to a local transformation of the root node directly, because it will be even more difficult for fanins with smaller (negative) slack to meet timing. The transformation(s) deployed during the recursive optimization of easier fanin pins may be shared with the difficult fanin pins, such that when the method processes the difficult fanin pins, their delays may have already been reduced from their original ones because of the shared transformation. This result is not achieved by working on the difficult fanin pins directly from the beginning. Therefore, this method leads to faster optimization, less area, and improved timing results.

Applicant respectfully submits that the citation of Figure 3.5 on page 45 does not describe "wherein reducing delays is performed recursively" as recited in **Claim 2**. The figure shows pseudo-code that has three steps and an end condition. There is nothing recursive in the cited pseudo-code.

Regarding the first element of **Claim 4**, Figure 3.1 on page 36 cited in Singh '92 does not describe "performing a timing analysis on a circuit", but rather it is about a decomposition method. Regarding the second element of Claim 4, equation 3.1 on page 47 cited in Singh '92 is about how much arrival time can be reduced, which is very different from "determining a delay target based at least in part on the timing analysis". Regarding the third element of Claim 4,

equation 3.2 on page 48 in Singh '92 calculates the achievable slack, while the slack value in the claim is the target to be achieved, which may not be achievable. The slack target at each node is calculated based on the overall circuit slack target. Regarding the fourth element of Claim 4, Applicant respectfully submits that the citation of page 50-51 (Proof) of Singh '92 does not describe "sorting the critical nodes based on the corresponding slack values." The proof cited at page 50 of Singh '92 proves a way to determine the maximum improvement and does not disclose the ordering technique as claimed.

Regarding **Claim 5** the "most critical output, O_1", cited on page 49 in Singh '92, is only used to determine the current worst slack, but is not used to order the critical outputs. However, "selecting a critical node having the largest negative slack" of the sorted critical nodes as claimed by Applicant orders the critical outputs to decide which one to start with for the recursive delay reduction process.

Regarding independent **Claim 6**, the arguments for Claims 1 and 2 apply here as well. As to dependent **Claim 7**, the arguments for Claim 1 apply here as well. Claim 7 again directed to ordering and in particular recites which node to start for delay reduction. The order impacts subsequent optimizations. Singh '92 does not provide any ordering techniques as claimed. Regarding **Claim 8**, lines 2-5 of page 51 in Singh '92 defines NON-critical nodes. In contrast, Applicant claims "performing a local transformation on the first node if the reducing delays for at least one of the critical fanins is not successful."

Regarding the first element of **Claim 9**, Figure 3.1 on page 36 cited in Singh '92 does not describe "performing a timing analysis on a circuit", but rather the figure is directed to a decomposition method. Regarding the second element of Claim 9, equation 3.1 on page 47 cited in Singh '92 is about how much arrival time can be reduced, which is very different from "determining a delay target based at least in part on the timing analysis". Regarding the third element of Claim 9, the "most critical output, O_1", cited on page 49 in Singh '92, is only used to determine the current worst slack. In contrast, Applicant has amended the third element to recite "selecting a first output having a negative slack based at least in part on the delay target <u>and the amount of first output negative slack relative to the slack of other outputs</u>". Regarding the fourth element of Claim 9 "performing local transformations on transitive fanins of the first output to improve the negative slack", this describes a recursive algorithm to reduce delay, that is, using

the delay reduction at transitive fanins of a node to reduce the delay of the current node. Lines 12-13 of page 49 in Singh '92, however, only identifies the possible candidates for transformation (which is the ε-critical netlist), and another algorithm is used to determine the transformations. These two methods are very different.

Regarding amended **Claim 11**, Applicant's first element, "identifying a first critical path between a first PI node and a first PO node, wherein the first critical path is selected based on ordering the PO nodes by corresponding slack values" is not described in Singh '92. As described above in conjunction with Claim 1, Singh does not select the first critical path based on ordering the PO nodes by corresponding slack values. Furthermore, Applicant's element g), "identifying a second critical path between a second PI node and a second PO node, wherein the second critical path is selected based on the ordered PO nodes" is also not described in Singh '92 for similar reasons.

Regarding **Claim 21**, Applicant's third element, "reducing a first critical path delay at a first node in closer proximity to a primary input associated with the critical path than to a node in closer proximity to the primary output", is not described in Singh '92. The method in Singh '92 does not prefer a transformation closer to the primary input. The citation of lines 4-12 on page 58 in Singh '92 indicates the opposite: it tries n1, closest to the primary output first, and only when it does not suffice, Singh '92 starts trying the transformation on n1's fanins. Applicant's fourth element, "storing the reduced delay", and fifth element "reducing a second critical path delay beginning at a second node located between the first node and the primary output based at least in part on the stored reduced delay", in one embodiment, refers to propagating the delay reduction during up and down moves along critical paths in a dynamic fashion. This is a significant differentiation in comparison with the disclosure of Singh '92. The Singh '92 reference describes pre-selecting a set of transformations while not considering their joint impact over each other.

Regarding **Claim 25**, in Singh '92 all outputs of the circuit have the same delay target, while Applicant's first and second elements, "selecting a desired circuit delay associated with a first output of a circuit path" and "calculating an initial circuit delay associated with the first output" allows different delay targets at different outputs, which is more practical for real designs and applications. Regarding the third element, Singh '92 uniformly reduces the circuit delay

along iterations, while Applicant claims "iteratively reducing the initial circuit delay to achieve the desired circuit delay using a timing optimization process, wherein in an iteration, mapping and clustering are used to measure the outcome of the timing optimization procedure, and wherein the timing optimization process uses such measurements to achieve the desired delay, and wherein the result of an iteration of delay reduction is used by a next iteration of delay reduction to determine an amount of delay to reduce" that dynamically determines the amount of delay to reduce based on the history of previous delay reduction iterations. Applicant's claimed method therefore yields better results compared to that achieved by the method described in Singh '92. Furthermore, Applicant respectfully submits that a portion of the third element: "using a timing optimization process, wherein in an iteration, mapping and clustering are used to measure the outcome of the timing optimization procedure, and wherein the timing optimization process uses such measurements to achieve the desired delay" is not described by the do/while loop of Figure 3.8 on page 50 of Singh '92.

Regarding amended **Claim 29**, the concept of depth 'd' is mentioned in Singh'88, but how to determine the value of d is unique in Applicant's claim. Applicant's claimed method can automatically or dynamically adjust the value of 'd' as opposed to using only one fixed value as described in the Singh'88 reference. The Singh'88 reference does not describe automatically changing the value of collapse depth if the value of the delay target is not met.

Therefore, Applicant respectfully requests the withdrawal of all claim rejections and prompt allowance of the claims.

Conclusion

In light of the above, reconsideration and withdrawal of the outstanding rejections are specifically requested. In view of the foregoing remarks, Applicant respectfully submits that the claims of the above-identified application are in condition for allowance. However, if the Examiner finds any impediment to allowing all claims that can be resolved by telephone, the Examiner is respectfully requested to call the undersigned.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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